

# DATA SHEET

## **74ALVCH16827**

20-bit buffer/line driver, non-inverting  
(3-State)

Product specification

1998 Jul 27

IC24 Data Handbook

## 20-bit buffer/line driver, non-inverting (3-State)

## 74ALVCH16827

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Wide supply voltage range of 1.2V to 3.6V
- CMOS low power consumption
- Direct interface with TTL levels
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparent, latched, clocked or clocked-enabled mode.
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- Current drive  $\pm 24$  mA at 3.0 V
- All inputs have bus hold circuitry
- Output drive capability 50 $\Omega$  transmission lines @ 85°C
- 3-State non-inverting outputs for bus oriented applications

## DESCRIPTION

The 74ALVCH16827 is a 20-bit non-inverting buffer/driver with 3-State outputs for bus oriented applications.

The 74ALVCH16827 consists of two 10-bit sections with separate output enable signals. For either 10-bit buffer section, the two output enable ( $1\overline{OE}1$  and  $1\overline{OE}2$  or  $2\overline{OE}1$  and  $2\overline{OE}2$ ) inputs must both be active. If either output enable input is high, the outputs of that 10-bit buffer section are in high impedance state.

The 74ALVCH16827 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay CP to Qn	$V_{CC} = 2.5\text{V}$ , $C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$	2.0 2.0	ns
$C_I$	Input capacitance		5	pF
$C_{PD}$	Power dissipation capacitance per latch	$V_I = \text{GND to } V_{CC}^1$	Output enabled 20 Output disabled 3	pF

## NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	74ALVCH16827 DGG	ACH16827 DGG	SOT364-1

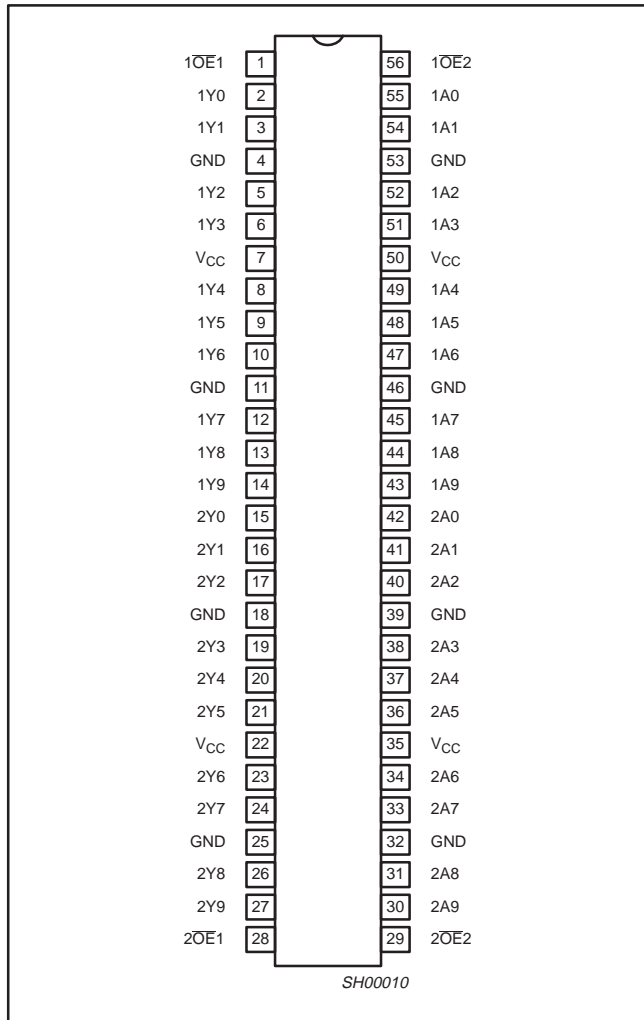
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 - 1A9 2A0 - 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 - 1Y9 2Y0 - 2Y9	Data outputs
1, 56, 28, 29	$1\overline{OE}0$ , $1\overline{OE}1$ $2\overline{OE}0$ , $2\overline{OE}1$	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	$V_{CC}$	Positive supply voltage

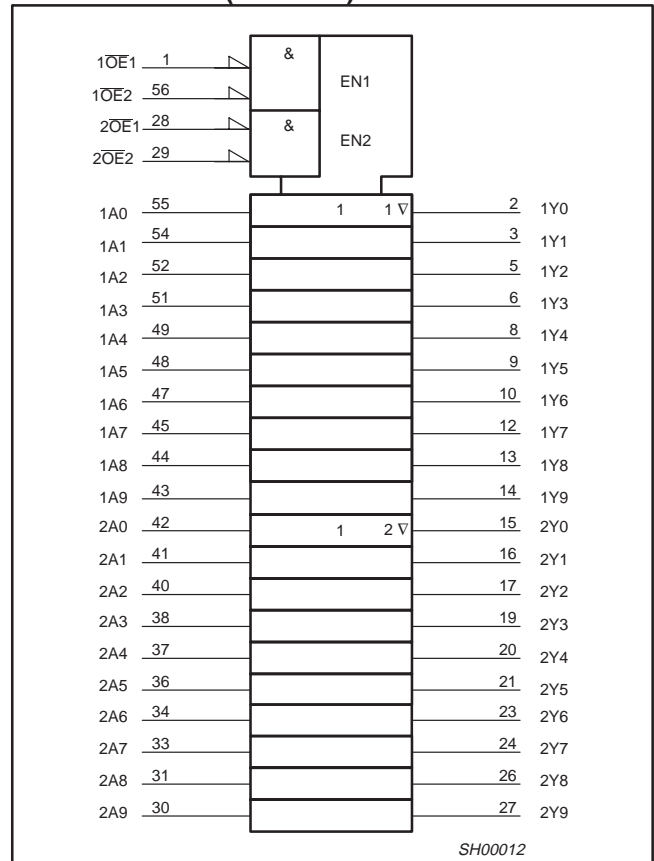
# 20-bit buffer/line driver, non-inverting (3-State)

# 74ALVCH16827

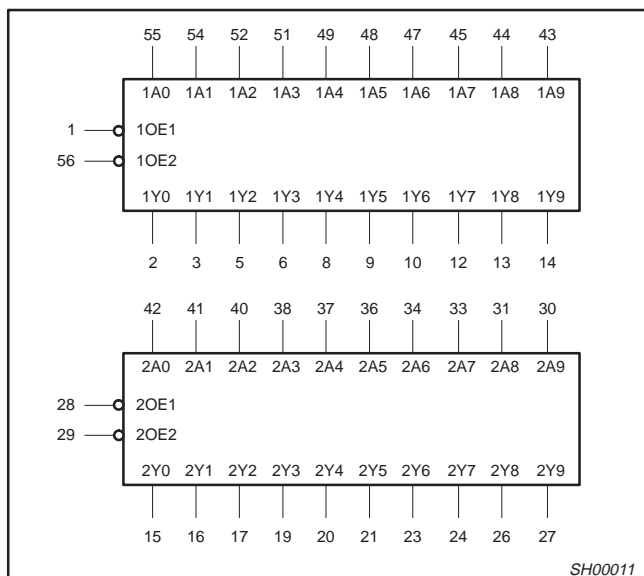
## PIN CONFIGURATION



## LOGIC SYMBOL (IEEE/IEC)



## LOGIC SYMBOL



## FUNCTION TABLE

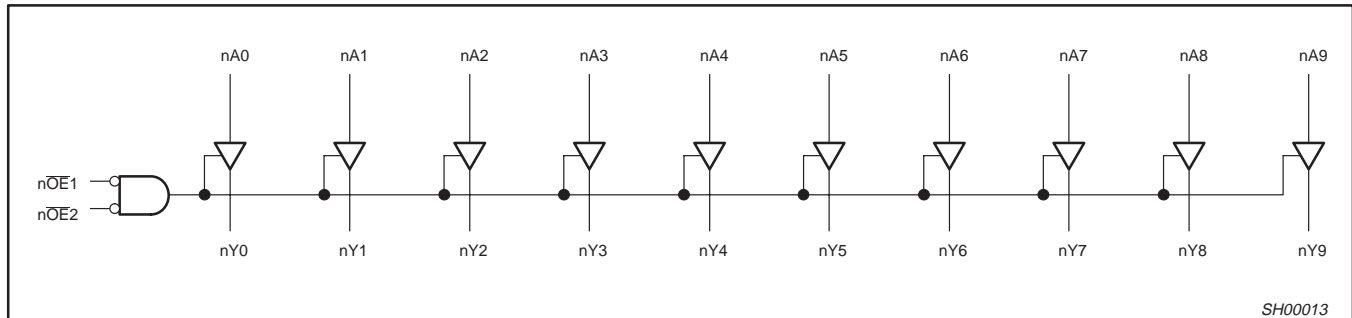
INPUTS			OUTPUTS
nOE1	nOE2	A	Y
L	L	L	L
L	L	H	H
H	H	X	Z
X	H	X	Z

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance "off" state

# 20-bit buffer/line driver, non-inverting (3-State)

# 74ALVCH16827

## LOGIC DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{CC}$	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
$V_I$	DC Input voltage range		0	$V_{CC}$	V
$V_O$	DC output voltage range		0	$V_{CC}$	V
$T_{amb}$	Operating free-air temperature range		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 2.3 \text{ to } 3.0\text{V}$	0	20	ns/V
		$V_{CC} = 3.0 \text{ to } 3.6\text{V}$	0	10	

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)  
 Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	For control pins <sup>2</sup>	-0.5 to +4.6	V
		For data inputs <sup>2</sup>	-0.5 to $V_{CC} + 0.5$	
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_O$	DC output voltage	Note 2	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		±100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package -plastic medium-shrink (SSOP) -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C	850 600	mW
		above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K		

### NOTE:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 20-bit buffer/line driver, non-inverting (3-State)

74ALVCH16827

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V	1.7	1.2		V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0	1.5		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V		1.2	0.7	V
		V <sub>CC</sub> = 2.7 to 3.6V		1.5	0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08		
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26		
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28		
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.07	0.40	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.15	0.70	V
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.14	0.40	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA		0.27	0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND		0.1	5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND		0.1	10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.2	40	μA
ΔI <sub>CC</sub>	Additional quiescent supply current	V <sub>CC</sub> = 2.3V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		150	750	μA
I <sub>BHL</sub> <sup>2</sup>	Bus hold LOW sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V	45	-		μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V	75	150		
I <sub>BHH</sub> <sup>2</sup>	Bus hold HIGH sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V	-45			μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V	-75	-175		
I <sub>BHLO</sub> <sup>2</sup>	Bus hold LOW overdrive current	V <sub>CC</sub> = 3.6V	500			μA
I <sub>BHHO</sub> <sup>2</sup>	Bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6V	-500			μA

**NOTES:**

1. All typical values are at T<sub>amb</sub> = 25°C.
2. Valid for data inputs of bus hold parts.

## 20-bit buffer/line driver, non-inverting (3-State)

74ALVCH16827

**AC CHARACTERISTICS FOR  $V_{CC} = 2.3V$  TO  $2.7V$  RANGE**GND = 0V;  $t_r = t_f \leq 2.0ns$ ;  $C_L = 30pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5 \pm 0.2V$			
			MIN	TYP <sup>1</sup>	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay nAn to nYn	1, 3	1.0	2.0	4.1	ns
$t_{PZH}/t_{PZL}$	3-State output enable time n $\bar{O}En$ to nYn	2, 3	1.0	2.9	6.0	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time n $\bar{O}En$ to nYn	2,3	1.2	2.1	5.6	ns

**NOTE:**1. All typical values are at  $V_{CC} = 2.5V$  and  $T_{amb} = 25^\circ C$ .**AC CHARACTERISTICS FOR  $V_{CC} = 3.0V$  TO  $3.6V$  RANGE AND  $V_{CC} = 2.7V$** GND = 0V;  $t_r = t_f \leq 2.5ns$ ;  $C_L = 50pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			$V_{CC} = 3.3 \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP <sup>1, 2</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay nAn to nYn	1, 3	1.0	2.0	3.4	1.0	2.1	3.9	ns
$t_{PZH}/t_{PZL}$	3-State output enable time n $\bar{O}En$ to nYn	2, 3	1.0	2.5	4.7	1.0	3.0	5.7	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time n $\bar{O}En$ to nYn	2, 3	1.3	2.8	4.5	1.3	3.1	4.9	ns

**NOTES:**1. All typical values are at  $V_{CC}$   $T_{amb} = 25^\circ C$ .2. Typical value is measured at  $V_{CC} = 3.3V$ .

# 20-bit buffer/line driver, non-inverting (3-State)

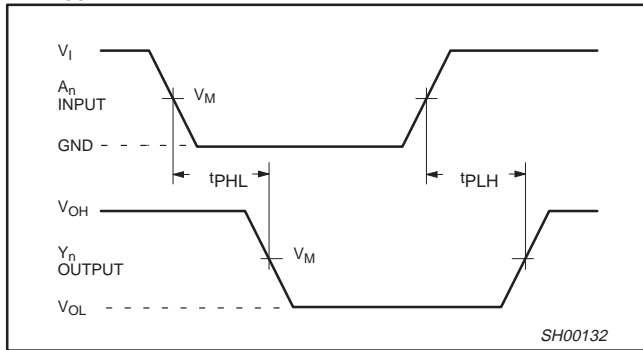
# 74ALVCH16827

### AC WAVEFORMS FOR $V_{CC} = 2.3V$ TO $2.7V$ AND $V_{CC} < 2.3V$ RANGE

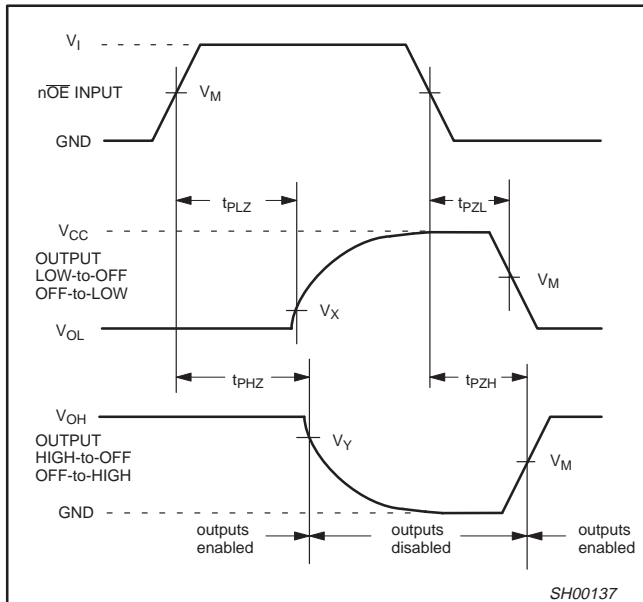
$V_M = 0.5 V$   
 $V_X = V_{OL} + 0.15V$   
 $V_Y = V_{OH} - 0.15V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

### AC WAVEFORMS FOR $V_{CC} = 3.0V$ TO $3.6V$ AND $V_{CC} = 2.7V$ RANGE

$V_M = 1.5 V$   
 $V_X = V_{OL} + 0.3V$   
 $V_Y = V_{OH} - 0.3V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = 2.7V$   
 $V_I = V_{CC}$



Waveform 1. The Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. The 3-State Output Enable and Disable Times

### TEST CIRCUIT

**Test Circuit for switching times**

**DEFINITIONS**  
 $R_L$  = Load resistor  
 $C_L$  = Load capacitance includes jig and probe capacitance  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**SWITCH POSITION**

TEST	$S_1$	$V_{CC}$	$V_I$
$t_{PLH}/t_{PHL}$	Open	< 2.7V	$V_{CC}$
$t_{PLZ}/t_{PZL}$	$2 * V_{CC}$	2.7-3.6V	2.7V
$t_{PHZ}/t_{PZH}$	GND		

SV00906

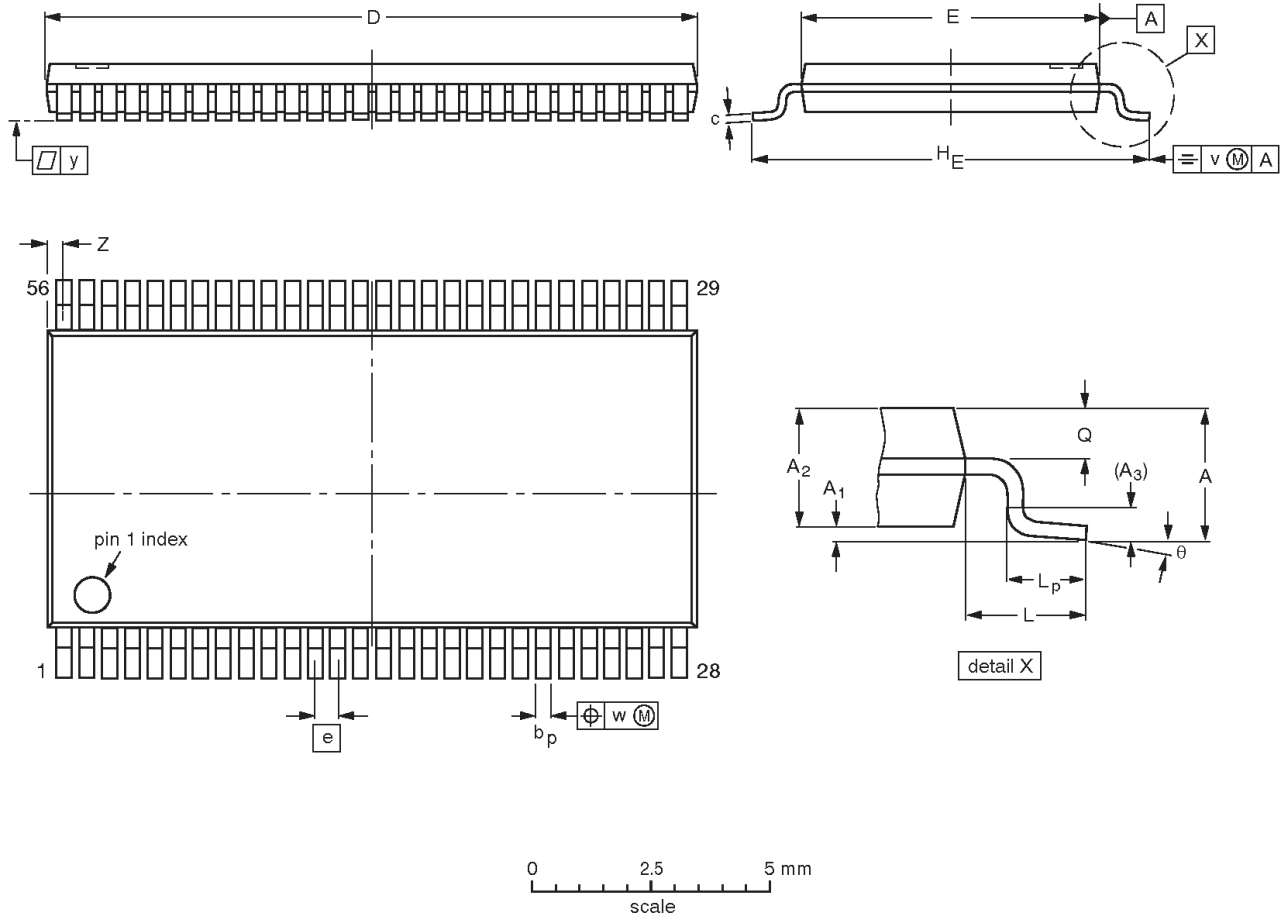
Waveform 3. Load circuitry for switching times

20-bit buffer/line driver, non-inverting (3-State)

74ALVCH16827

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				93-02-03 95-02-10



---

20-bit buffer/line driver, non-inverting (3-State)

74ALVCH16827

---

**NOTES**

## 20-bit buffer/line driver, non-inverting (3-State)

74ALVCH16827

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1998  
All rights reserved. Printed in U.S.A.

print code

Date of release: 08-98

Document order number:

9397-750-04556

*Let's make things better.*